SONY

1/3-inch CCD Image Sensor for CCIR B/W Camera

Description

The ICX059AL is an interline transfer CCD solid state image sensor suitable for CCIR B/W video cameras. High sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

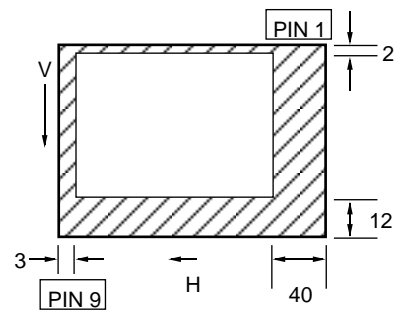16 pin DIP (CERDIP)   16 pin DIP (Plastic)

Features

• High image, high sensitivity and low dark current
• Consecutive various speed shutter 1/50s (typ.),1/120s to 1/10,000s
• Low smear
• High anti-blooming
• Horizontal register 5V drive
• Reset gate 5V drive

Device Structure

• Optical size: 1/3 inch format
• Number of effective pixels: 752 (H) x 582 (V), approx. 440k pixels
• Number of total pixels: 795 (H) x 596 (V), approx. 470k pixels
• Interline transfer CCD image sensor
• Chip size: 6.00mm (H) x 4.96mm (V)
• Unit cell size: 6.5μm (H) x 6.25μm (V)
• Optical black: Horizontal (H) direction: Front 3 pixels, Rear 40 pixels
  Vertical (V) direction: Front 12 pixels, Rear 2 pixels
• Number of dummy bits: Horizontal: 22
  Vertical: 1 (even field only)
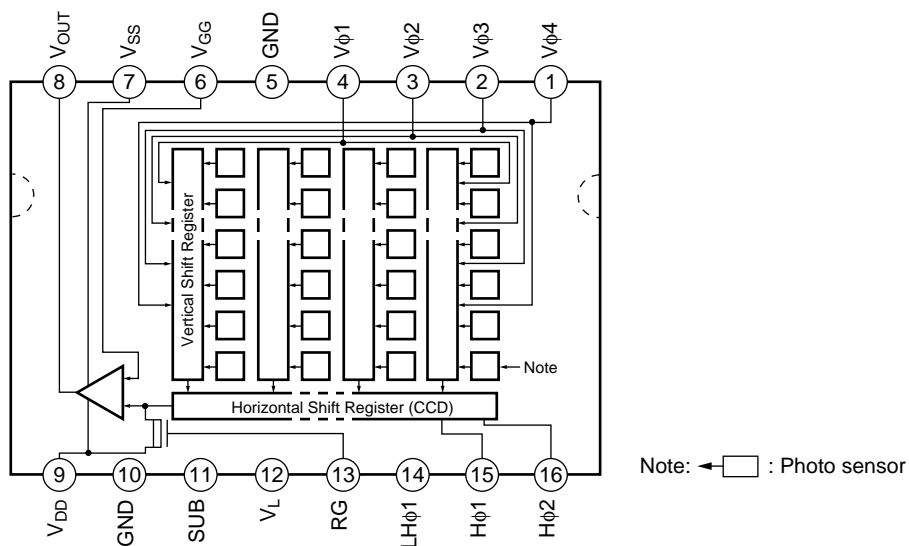• Board material: N-type silicon
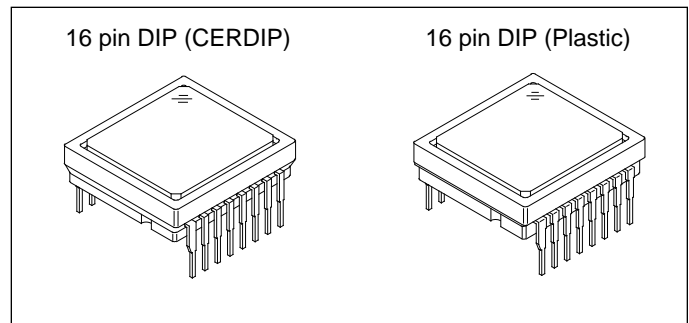
Optical Black Position (Top View)

PIN 1

V

2

3

PIN 9

H

40

12

E92202B56–ST

Block Diagram (Top View)

Note: ◄▭ : Photo sensor

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	9	VDD	Output amplifier drain supply
2	Vφ3	Vertical register transfer clock	10	GND	Ground
3	Vφ2	Vertical register transfer clock	11	SUB	Substrate (Overflow drain)
4	Vφ1	Vertical register transfer clock	12	VL	Protective transistor bias
5	GND	Ground	13	RG	Reset gate clock
6	VGG	Output amplifier gate bias	14	LHφ1	Horizontal register final stage transfer clock
7	VSS	Output amplifier source	15	Hφ1	Horizontal register transfer clock
8	VOUT	Signal output	16	Hφ2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB–GND		−0.3 to +55	V	
Supply voltage	VDD, VOUT, VSS – GND	−0.3 to +18	V	
	VDD, VOUT, VSS – SUB	−55 to +10	V	
Vertical clock	Vφ1, Vφ2, Vφ3, Vφ4 – GND	−15 to +20	V	
input voltage	Vφ1, Vφ2, Vφ3, Vφ4 – SUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	Note 1
Voltage difference between horizontal clock input pins		to +17	V	
Hφ1, Hφ2–Vφ4		−17 to +17	V	
Hφ1, Hφ2, LHφ1, RG, VGG–GND		−10 to +15	V	
Hφ1, Hφ2, LHφ1, RG, VGG–SUB		−55 to +10	V	
VL–SUB		−65 to +0.3	V	
Vφ1, Vφ2, Vφ3, Vφ4, VDD, VOUT–VL		−0.3 to +30	V	
RG–VL		−0.3 to +24	V	
VGG, VSS, Hφ1, Hφ2, LHφ1–VL		−0.3 to +20	V	
Storage temperature		−30 to +80	°C	
Operating temperature		−10 to +60	°C	

NOTE:

1. +27V (max.) when clock width <10μs, duty factor <0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	3.8	4.2	4.65	V	
Output amplifier source	V_{SS}	Ground Through 820Ω resistor				±5 %
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	Note 2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	Notes 2, 6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	Note 3				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	µA	Note 4
Input current	I_{IN2}			10	µA	Note 5

NOTES:

2. Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
   Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ±3%.

   V_{SUB} code address–1 digit display

   V_{RGL} code address–1 digit display

   V_{SUB} address code
   V_{RGL} address code
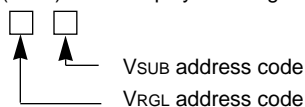
   Code addresses and actual numerical values correspond to each other as follows:

V_{RGL} Address Code	1	2	3	4	5	6	7
Numerical Value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} Address Code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical Value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

   <Example> "5L" → V_{RGL} = 3.0V
   V_{SUB} = 12.0V

3. V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.
4. a. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, V_{SS} and SUB pins, while pins that are not tested are grounded .
   b. Current to each pins when 20V is applied sequentially to $V\phi1$, $V\phi2$, $V\phi3$ and $V\phi4$, while pins that are not tested are grounded. However, 20V is applied to SUB.
   c. Current to each pins when 15V is applied sequentially to pins RG, $LH\phi1$, $H\phi1$, $H\phi2$ and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
   d. Apply 30V to pins $V\phi1$, $V\phi2$, $V\phi3$, $V\phi4$, V_{DD}, V_{OUT}; 24V to Pin RG; and 20V to pins V_{GG}, V_{SS}, $H\phi1$, $H\phi2$, $LH\phi1$. The above is the current that flows to Pin V_L when it is grounded. Please note that pins GND and SUB are to be disconnected.
5. Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

| Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	−0.05	0	0.05	V	2	V_{VH} = (V_{VH1}+V_{VH2}) /2
	V_{VH3}, V_{VH4}	−0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	−9.0	−8.5	−8.0	V	2	V_{VL} = (V_{VL3}+V_{VL4}) /2
	$V_{\phi V}$	7.8	8.5	9.05	V	2	$V_{\phi V}$ = (V_{VHn}+V_{VLn}) (n = 1 to 4)
	$\vert V_{VH1}-V_{VH2} \vert$			0.1	V	2	
	$V_{VH3}-V_{VH}$	−0.25		0.1	V	2	
	$V_{VH4}-V_{VH}$	−0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$, $V_{\phi LH}$	4.75	5.0	5.25	V	3	Note 6
	V_{HL}, V_{LHL}	−0.05	0	0.05	V	3	Note 6
Reset gate clock voltage	$V_{\phi RG}$	4.5	5.0	5.5	V	4	Note 7
	$V_{RGLH}-V_{RGLL}$			0.8	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	22.5	23.5	24.5	V	5	

NOTES:
6. The horizontal final stage transfer clock input pin LHφ1 is connected to the horizontal transfer clock input pin Hφ1.
7. No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Reset gate clock voltage	V_{RGL}	−0.2	0	0.2	V	4	
	$V_{\phi RG}$	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1$, $C\phi V3$		1000		pF	
	$C\phi V2$, $C\phi V4$		560		pF	
Capacitance between vertical transfer clocks	$C\phi V12$, $C\phi V34$		470		pF	
	$C\phi V23$, $C\phi V41$		390		pF	
	$C\phi V13$		180		pF	
	$C\phi V24$		100		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1$, $C\phi H2$		47		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		51		pF	
Capacitance between horizontal final stage transfer clock and GND	$C\phi LH$		8		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		8		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		270		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi H$		15		Ω	

Vertical Transfer Clock Equivalent Circuit
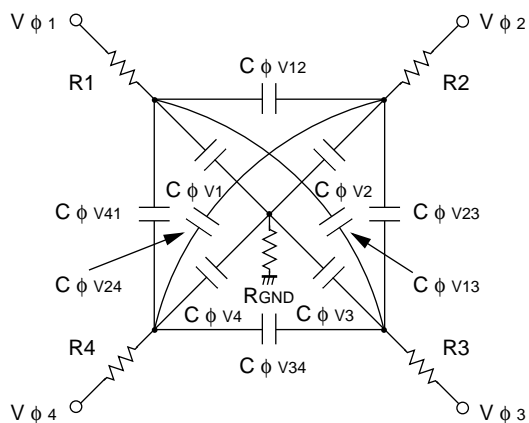
Horizontal Transfer Clock Equivalent Circuit
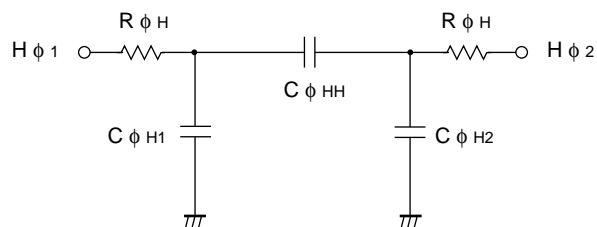
Drive Clock Waveform Conditions

(1) Readout Clock Waveform

100%
90%

ϕM

V_{VT}

$\dfrac{\phi M}{2}$

10%
0%

0V

t_r t_{wh} t_f

(2) Vertical Transfer Clock Waveform

Vϕ1

V_{VH1} V_{VHH} V_{VH} V_{VHH}
V_{VHL}
V_{VHL}
V_{VL1} V_{VLH}
V_{VLL}
V_{VL}

Vϕ3

V_{VHH} V_{VHH} V_{VH}
V_{VHL} V_{VHL}
V_{VH3}
V_{VL3} V_{VLH}
V_{VLL}
V_{VL}

Vϕ2

V_{VHH} V_{VHH} V_{VH}
V_{VHL}
V_{VH2} V_{VHL}
V_{VL2} V_{VLH}
V_{VL} V_{VLL}

Vϕ4

V_{VH} V_{VHH} V_{VHH}
V_{VHL} V_{VHL}
V_{VH4}
V_{VLH}
V_{VLL}
V_{VL4} V_{VL}
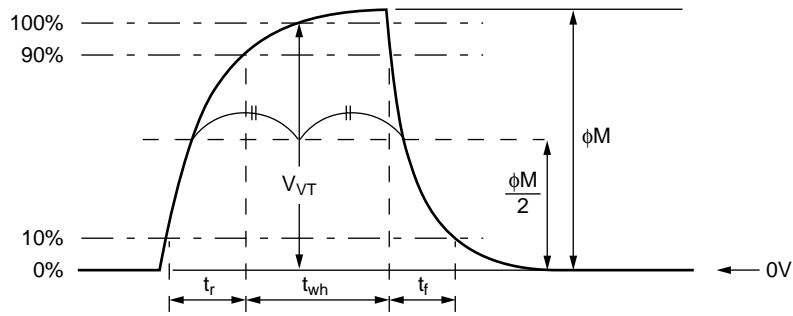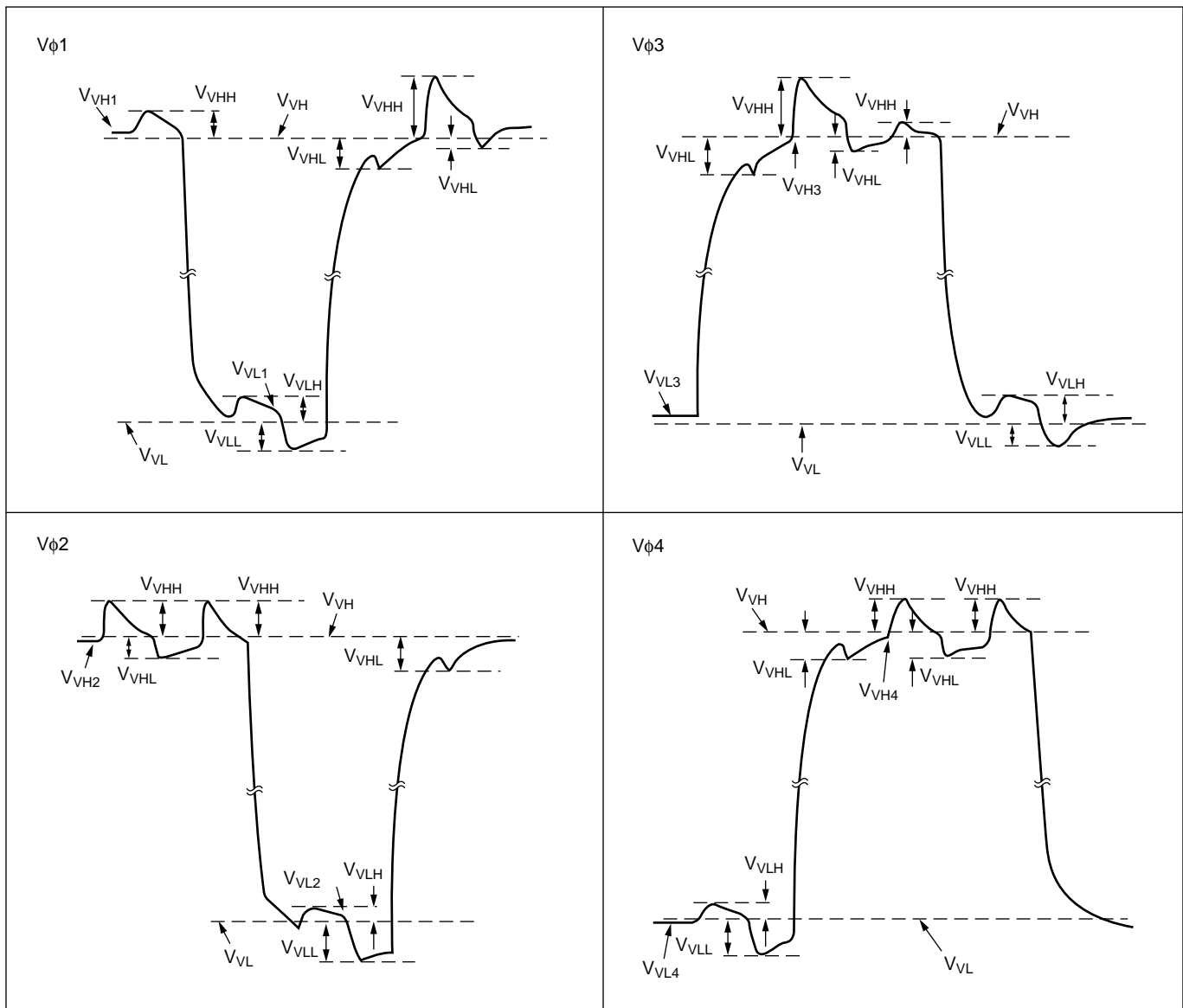
NOTES:
$V_{VH} = (V_{VH1} + V_{VH2})/2$
$V_{VL} = (V_{VL3} + V_{VL4})/2$
$V\phi V = V_{VHn} - V_{VLn}$ (n = 1 to 4)

(3) Horizontal Transfer Clock Waveform Diagram
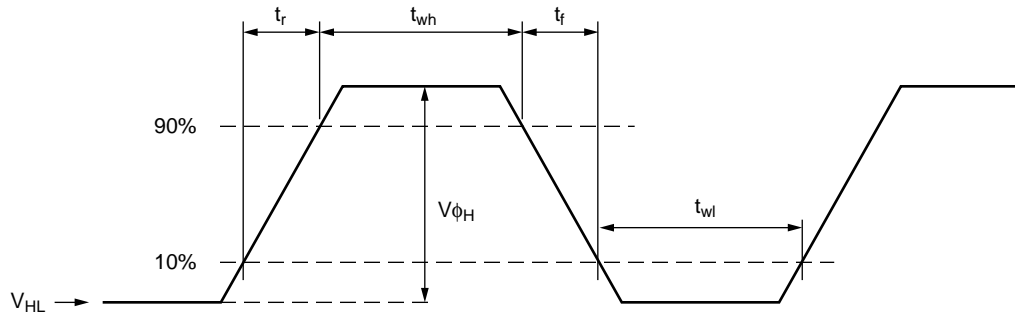
(4) Reset Gate Clock Waveform Diagram
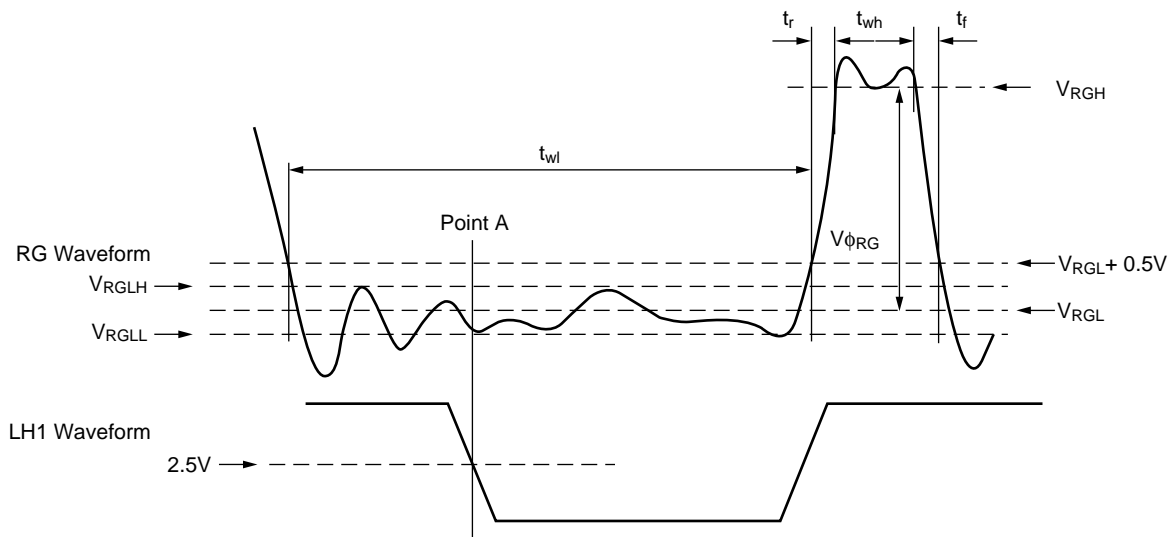
    V$_{RGLH}$ is the maximum value and V$_{RGLL}$ is the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.
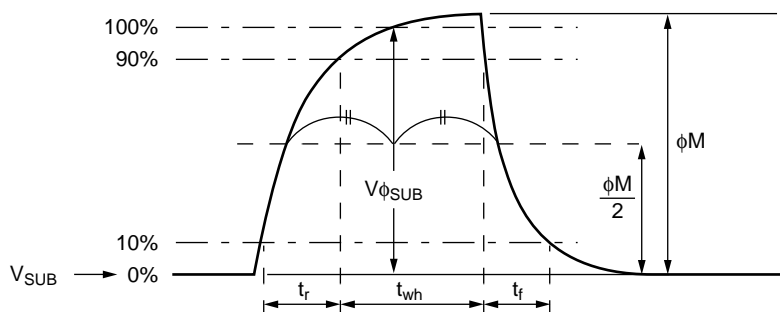
    V$_{RGL}$ is the mean value for V$_{RGLH}$ and V$_{RGLL}$.

$$V_{RGL} = (V_{RGLH}+V_{RGLL})/2$$

    V$_{RGH}$ is the minimum value for twh period.

$$V\phi_{RG} = V_{RGH}-V_{RGL}$$

(5) Substrate Clock Waveform

Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5						0.5			0.5		μs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										15		250	ns	Note 8
Horizontal transfer clock	$H\phi_1$, $LH\phi_1$	18	24		19.5	26			10	17.5		10	17.5	ns	Note 9
During Imaging	$H\phi_2$	21	26		19	24			10	15		10	15	ns	
Hoizontal transfer clock	$H\phi_1$, $LH\phi_1$		6.41						0.01			0.01		μs	
During parallel serial conversion	$H\phi_2$					6.41			0.01			0.01		μs	
Reset gate clock	ϕRG	11	13			51			3			3		ns	
Substrate clock	ϕSUB	1.5	1.8							0.5			0.5	μs	During charge drain

NOTES:

8. When vertical transfer clock driver CXD1250 is in use.

9. tf ≥ tr−2ns, and the crosspoint voltage (V_{CR}) of the $H\phi_1 \cdot LH\phi_1$ rise side of waveforms $H\phi_1 \cdot LH\phi_1$ and $H\phi_2$ must be at least 2.5V.

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1 \cdot LH\phi_1$, $LH\phi_2$	16	20		ns	Note 10

NOTES:

10. "two" is the overlap period of horizontal transfer clocks $H\phi_1 \cdot LH\phi_1$ and $H\phi_2$'s twh and twl.

11. Because the horizontal final stage transfer clock $LH\phi_1$ is connected to the horizontal transfer clock $H\phi_1$, specifications will be the same as $H\phi_1$.

Operating Characteristics

(Ta = +25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Method	Remarks
Sensitivity	S	240	300		mV	1	
Saturation signal	Vsat	540			mV	2	Ta = +60°C
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta = +60°C
Dark signal shading	∆Vdt			1	mV	6	Ta = +60°C
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Chart of Video Signal Shading
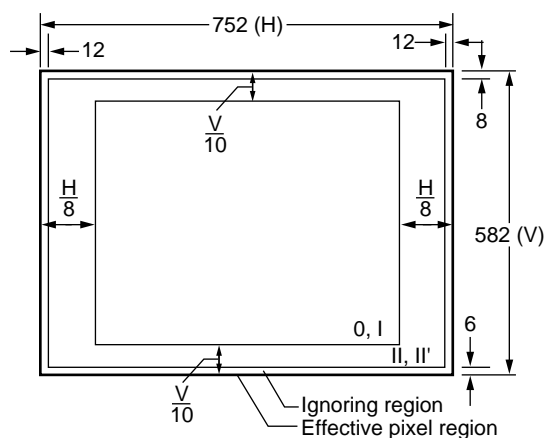
Image Sensor Characteristics Test Method

Test Conditions

① Through the following tests, the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests, defects are excluded and, unless otherwise specified, the optical black level (henceforth referred to as OB) is set as the reference, the values obtained at Ⓐ point in the figure at the Drive Circuit are utilized.

Image Sensor Characteristics Test Method

Definition of Standard Imaging Conditions

① Standard Imaging Condition I: (as imaging device) Use a pattern box (luminance 706cd/m2, color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity.

② Standard Imaging Condition II: Image a light source (color temperature of 3200K) whose uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity

   Set to Standard Imaging Condition I. After selecting the electronic shutter mode at a 1/250s shutter speed, measure the signal output (Vs) at the center of the screen and substitute in the following formula.

   $$S = Vs \times \frac{250}{60} \text{ [mV]}$$

2. Saturation signal

   Set to Standard Imaging Condition II. Adjust light intensity to 10 times that of signal output average value (V_A = 200mV), then test signal minimum value.

3. Smear

   Set to Standard Imaging Condition II. Adjust light intensity to 500 times that of signal output average value (V_A = 200mV) with lens diaphragm at F5.6 to F8. Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value VSm [mV] of Y signal output.

   $$Sm = \frac{VSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ (\%)(1/10V)}$$

4. Video signal shading

   Set to Standard Imaging Condition II. Adjust light intensity to signal output average value (V = 200mV) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax [mV]) and minimum (Vmin [mV]) values of signal output.

   $$SH = (Vmax - Vmin) / 200 \times 100 \text{ (\%)}$$

5. Dark signal

   Test signal output average value Vdt [mV] when the device ambient temperature is at +60°C and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading

   Following 5, test maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of dark signal output.

   $$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

7. Flicker

   Set to Standard Imaging Condition II. Adjust light intensity to signal output average value (V_A = 200mV). Then test the V signal difference (ΔVf [mV]) between even field and odd field.

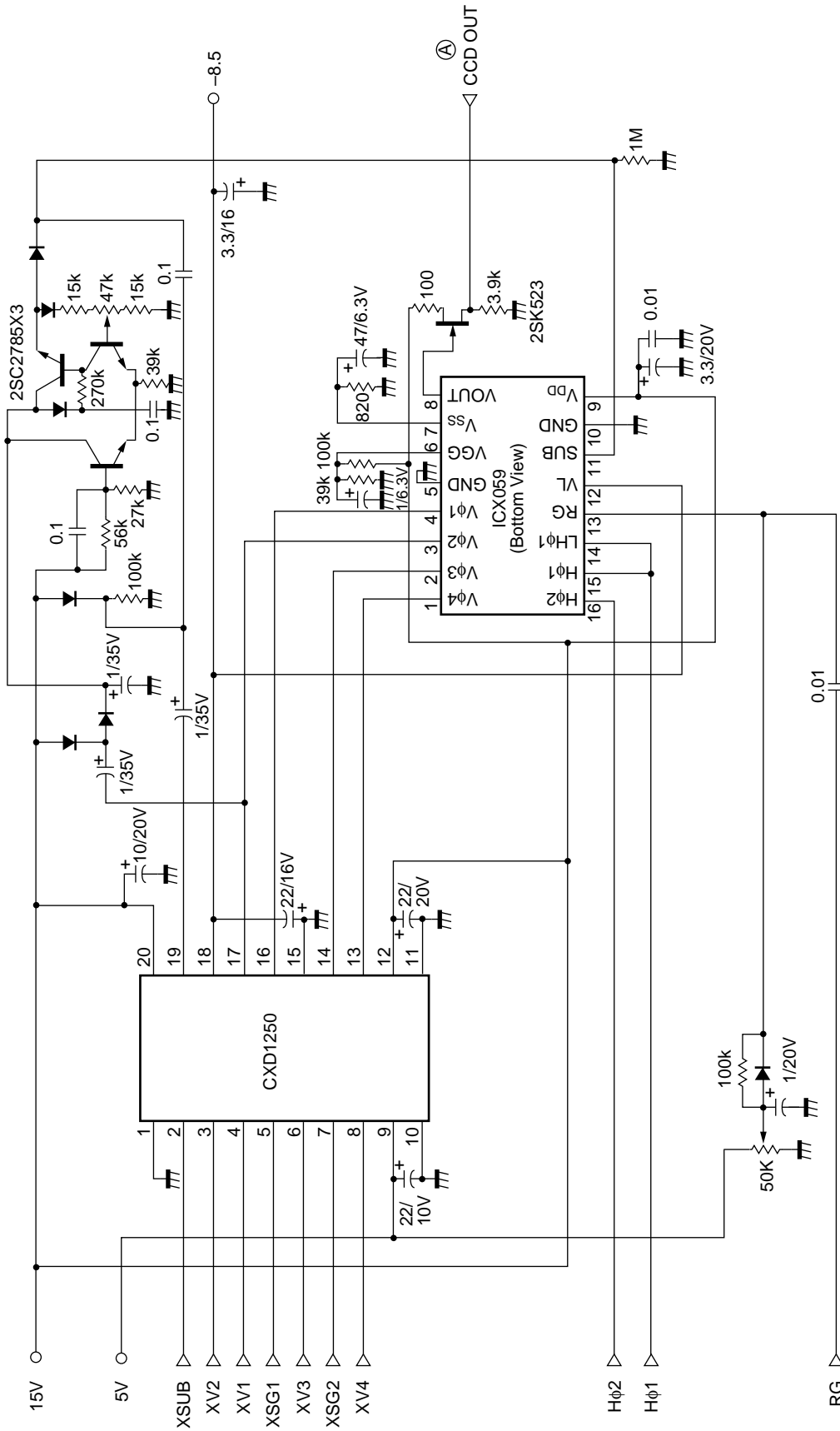 $$F = (\Delta Vf / 200) \times 100 \text{ (\%)}$$

8. Residual image

   Adjust V signal output value by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag/200) x 100 (%)

FLD

SG1

Light

Strobe light timing

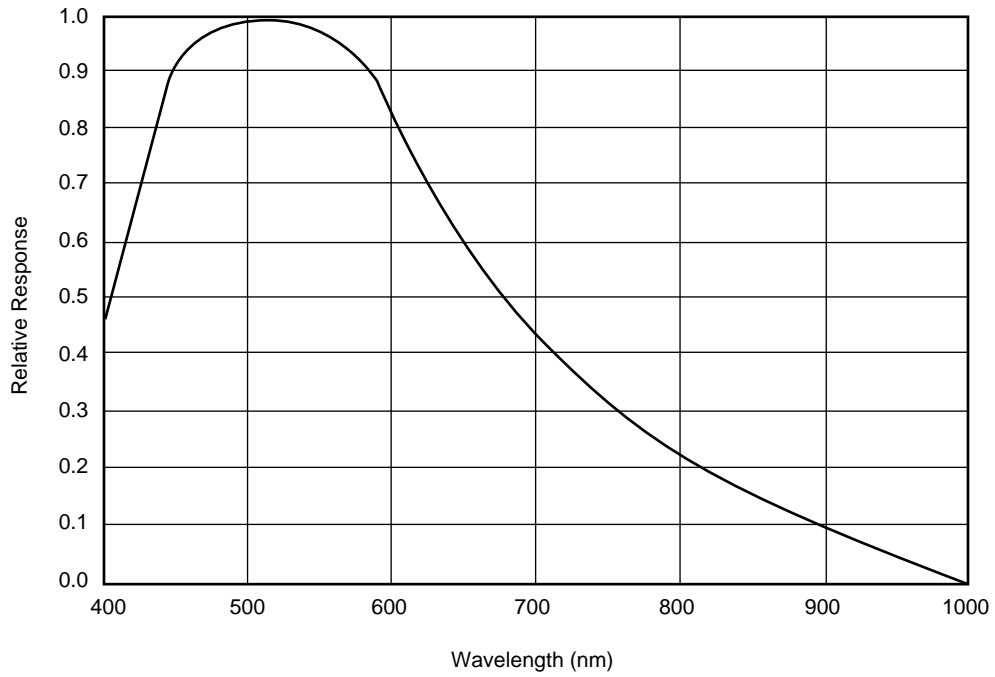Output signal
200mV
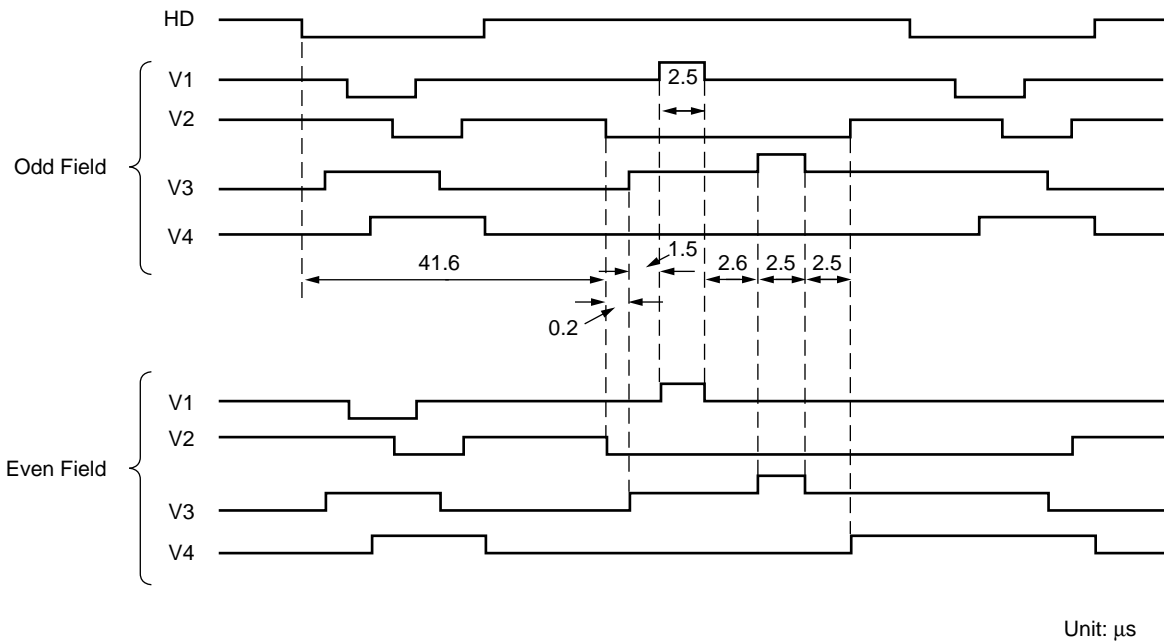
Vlag (Residual image)

Output
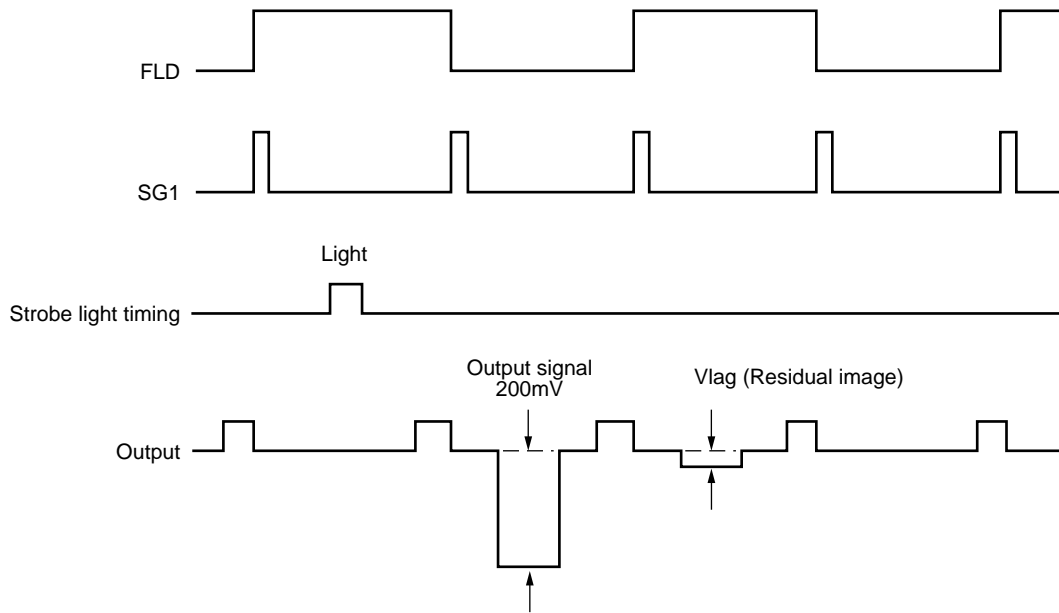
Drive Circuit
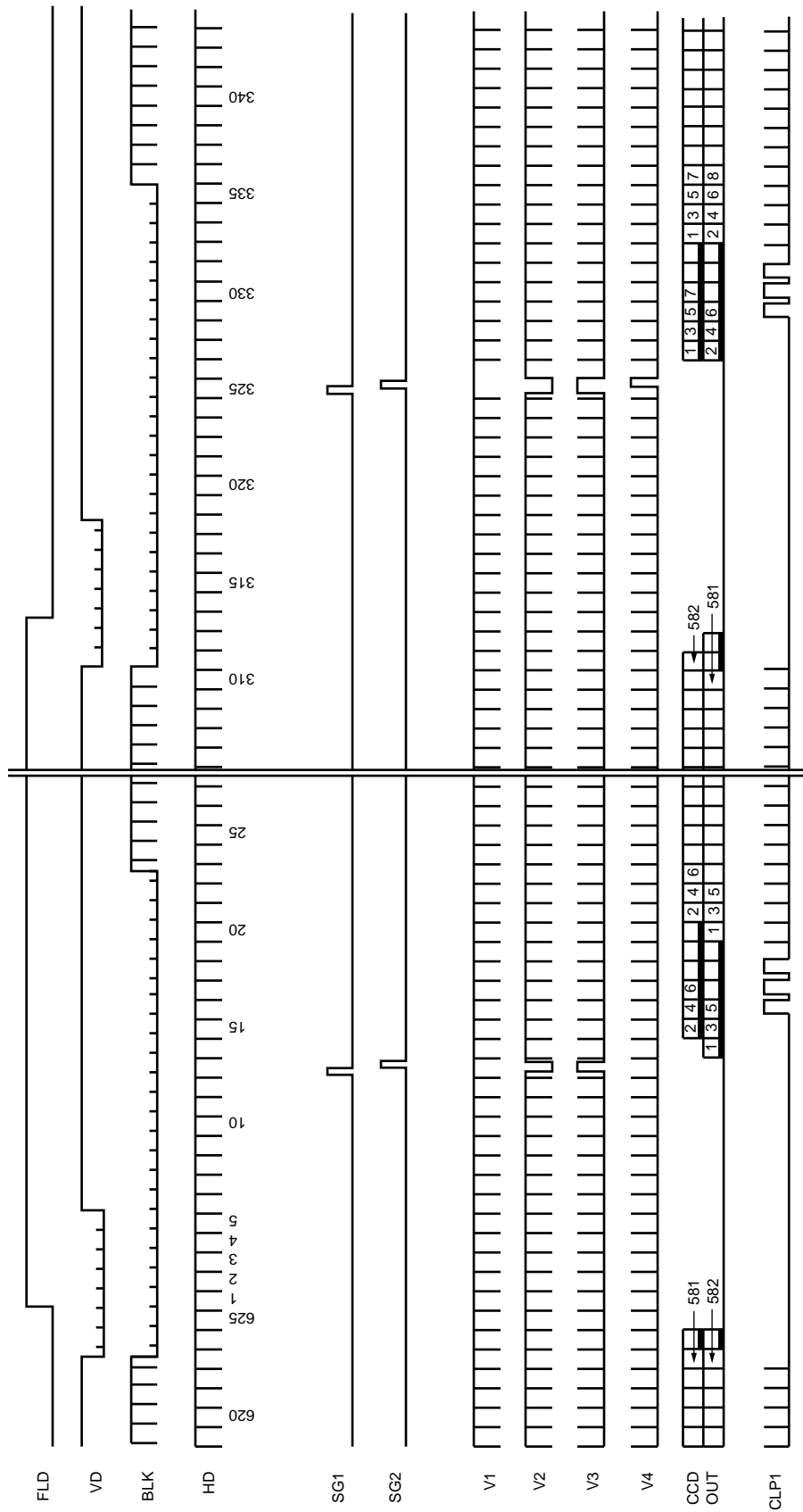
Spectral Sensitivity Characteristics

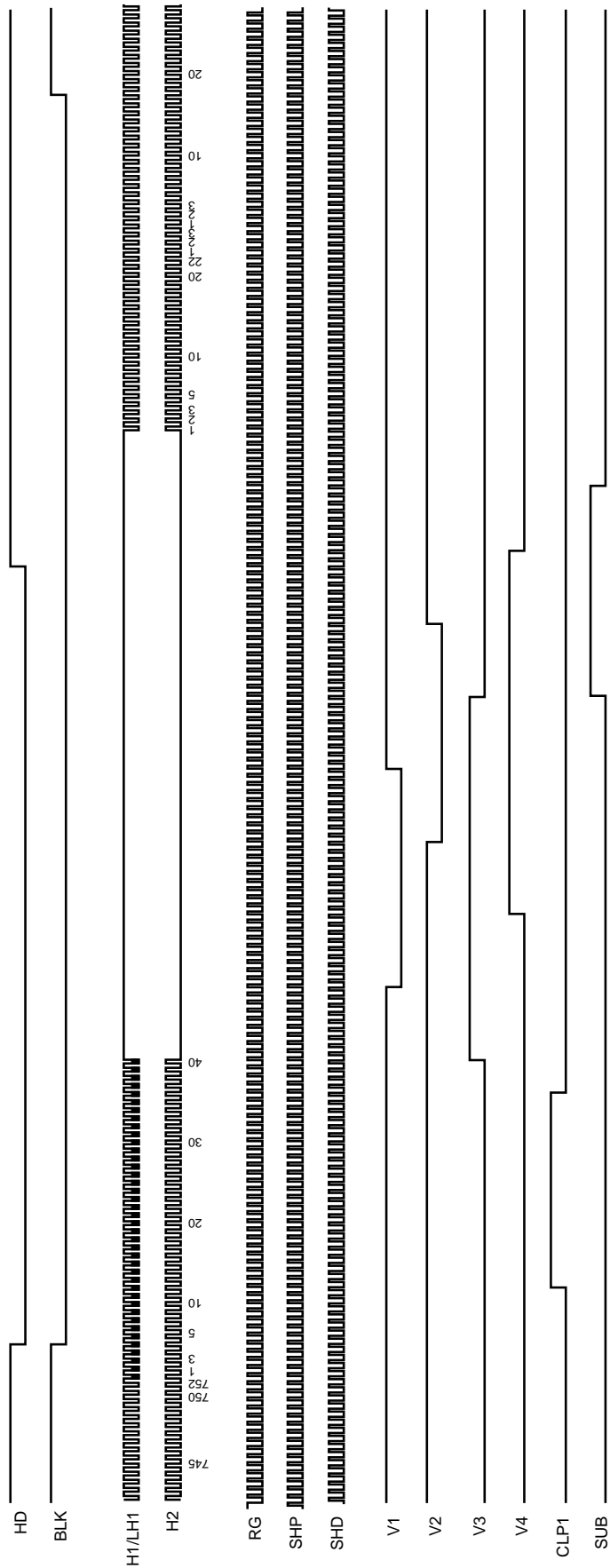(Excluding light source characteristics, including lens characteristics)

Using Read Out Clock Timing Chart

Unit: µs

Drive Timing Chart (Vertical Sync)

Drive Timing Chart (Horizontal Sync)

Notes on Handling

1. Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling, be sure to take the following protective measures:

a)   Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.

b)   When handling directly, use a grounding band.

c)   Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d)   Ionized air is recommended for discharge when handling CCD image sensors.

e)   For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2. Soldering

a)   Make sure the package temperature does not exceed +80°C.

b)   Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c)   To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3. Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting their glass plates from harmful dust and dirt. Clean glass plates with the following operation:

a)   Operate in clean environments (around class 1000 is appropriate).

b)   Do not touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity, ionized air is recommended.)

c)   Clean with a cotton swab and ethyl alcohol if grease stained. Be careful not to scratch the glass.

d)   Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

e)   When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4. Light resistance

B/W image sensor: Do not expose to strong light (sun rays) for long periods. For continuous use under adverse conditions exceeding the normal use conditions, consult Sony Semiconductor.

Color image sensor: Do not expose to strong light (sun rays) for long periods. Color filters will be discolored. For continuous use under adverse conditions exceeding the normal use conditions, consult Sony Semiconductor.

5. Exposure to high temperature or humidity will affect the characteristics. Accordingly, avoid storage or usage in such conditions.

6. CCD image sensors are precise optical equipment that should not be subjected to a high incidence of mechanical shocks.

Package Outline (CERDIP)   Unit: mm

16 pin DIP (450mil)
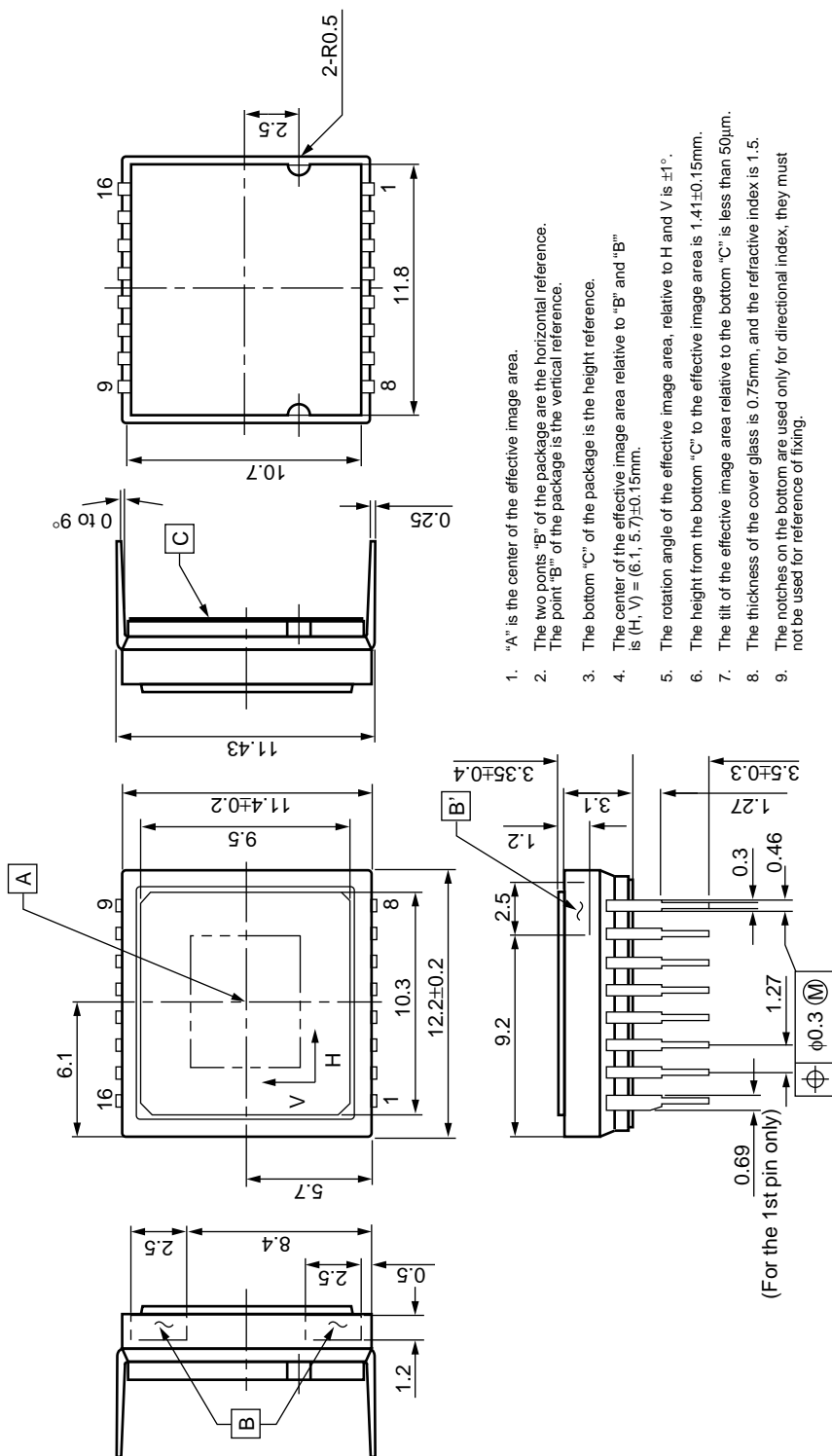
1. "A" is the center of the effective image area.
2. The two ponts "B" of the package are the horizontal reference.
    The point "B'" of the package is the vertical reference.
3. The bottom "C" of the package is the height reference.
4. The center of the effective image area relative to "B" and "B'"
    is (H, V) = (6.1, 5.7)±0.15mm.
5. The rotation angle of the effective image area, relative to H and V is ±1°.
6. The height from the bottom "C" to the effective image area is 1.41±0.15mm.
7. The tilt of the effective image area relative to the bottom "C" is less than 50µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notches on the bottom are used only for directional index, they must
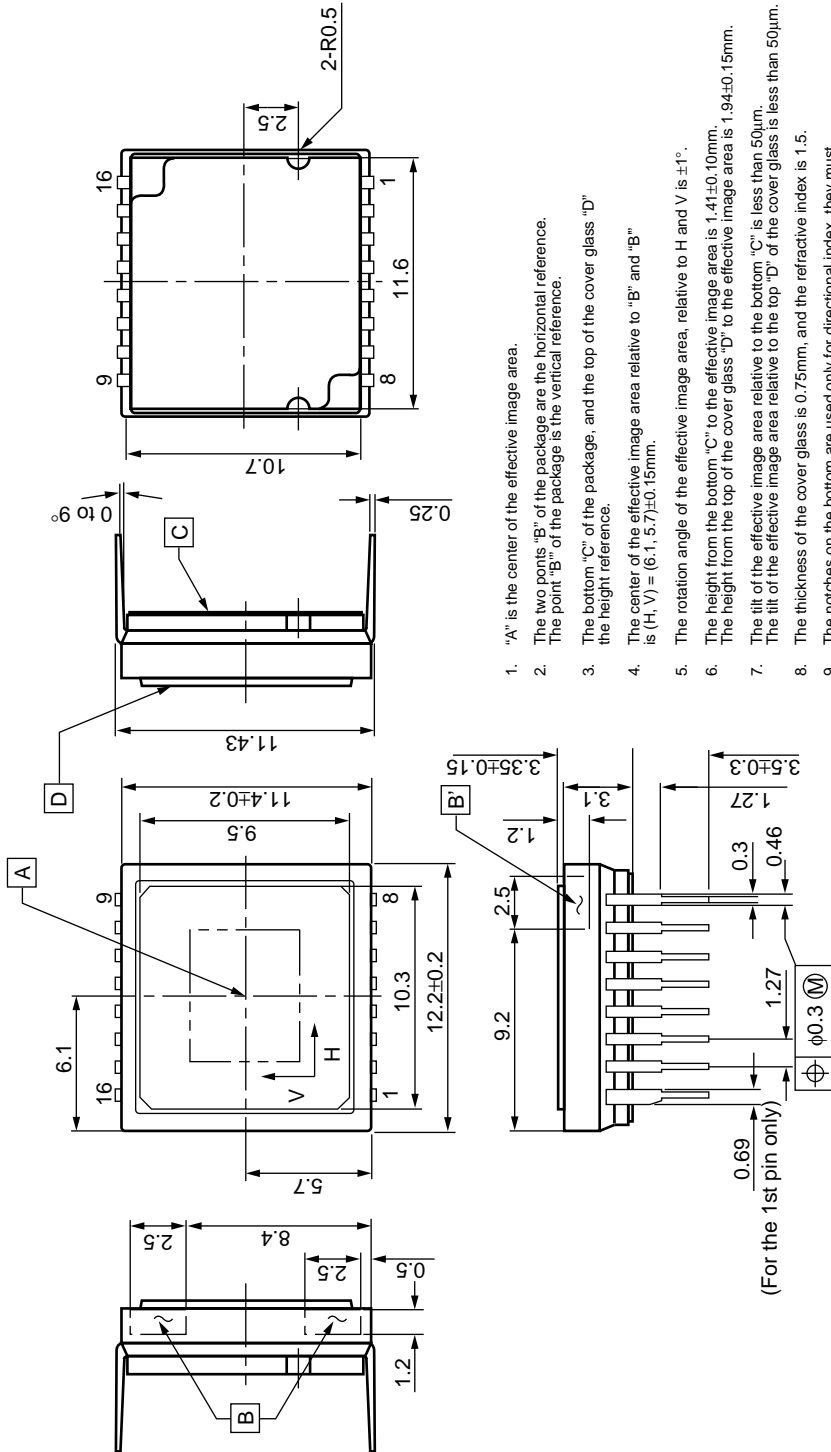   not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.2g

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Planned from the production of April, 1995.

Package Outline (Plastic)   Unit: mm

16 pin DIP (450mil)

1. "A" is the center of the effective image area.

2. The two ponts "B" of the package are the horizontal reference.
    The point "B" of the package is the vertical reference.

3. The bottom "C" of the package, and the top of the cover glass "D"
    the height reference.

4. The center of the effective image area relative to "B" and "B"
    is (H, V) = (6.1, 5.7)±0.15mm.

5. The rotation angle of the effective image area, relative to H and V is ±1°.

6. The height from the bottom "C" to the effective image area is 1.41±0.10mm.
    The height from the top of the cover glass "D" to the effective image area is 1.94±0.15mm.

7. The tilt of the effective image area relative to the bottom "C" is less than 50μm.
    The tilt of the effective image area relative to the top "D" of the cover glass is less than 50μm.

8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.

9. The notches on the bottom are used only for directional index, they must
    not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.9g

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